CLAIMS

Claims 1-15 are currently pending in the application. Claim 1 is an independent claim and claims 2-15 depend there from.

1. (Previously Presented) A system for reducing noise in a chip, the system comprising:

a substrate layer integrated within the chip;

a transistor layer integrated within the chip, which is shielded from said substrate layer by a shielding layer;

at least one transistor of a first transistor type that couples said transistor layer to said shielding layer; and

a positive potential of a quiet voltage source that is coupled to said at least one transistor of said first transistor type.

2. (Original) The system according to claim 1, further comprising at least one transistor of a second transistor type coupled to said shielding layer.

3. (Previously Presented) The system according to claim 2, wherein said at least one transistor of said second transistor type is an n-type transistor.

4. (Previously Presented) The system according to claim 2, wherein said at least one transistor of said second transistor type is disposed within said transistor layer.

5. (Previously Presented) The system according to claim 2, wherein said at least one transistor of said second transistor type is resistively coupled to said shielding layer.

6. (Previously Presented) The system according to claim 2, further comprising a first noisy voltage source coupled to said at least one transistor of said second transistor type.

7. (Previously Presented) The system according to claim 6, wherein said first noisy voltage source is coupled to a source of said at least one transistor of said second transistor type.

8. (Previously Presented) The system according to claim 1, wherein said at least one transistor of said first transistor type is a p-type.

9. (Previously Presented) The system according to claim 1, wherein said at least one transistor of said first transistor type is disposed within said transistor layer.

10. (Previously Presented) The system according to claim 1, wherein said at least one transistor of said first transistor type is capacitively coupled to said shielding layer.

11. (Original) The system according to claim 1, wherein said shielding layer is capacitively coupled to said substrate layer.

12. (Original) The system according to claim 1, wherein said shielding layer is disposed between said substrate layer and said transistor layer.

13. (Original) The system according to claim 1, wherein said shielding layer is a deep N-well.

14. (Previously Presented) The system according to claim 1, further comprising a noisy voltage source coupled to said at least one transistor of a first transistor type.

15. (Previously Presented) The system according to claim 14, wherein said noisy voltage source is coupled to a source of said at least one transistor of a first transistor type.